REMARKS

Reconsideration of the present application is respectfully requested in view of the following comments.

1. Interview of December 10, 2003

Applicant appreciates the courtesy of the Examiner in granting an interview with Applicant's representative on December 10, 2003. In accordance with the discussion at the interview, Applicant submits new claims and presents commentary discussing the distinguishing characteristics of the present invention over the cited prior art in view of the new claims.

2. New Claims 11-18

During the interview, the pending claims of the present application and language used in possible new claims were discussed at length.

Figures 1a-1h of the present application were used to devise the new claims. More specifically, the various steps shown in the figures have thus been incorporated in new claims 11 and 18.

It was suggested during the interview that the vertical contacts should be distinguished to avoid any confusion in the steps of forming the vertical contacts. As is now evident, first and second side vertical contacts are recited in the claims, and clearly are described and shown in the application as filed.

It was discussed that previously presented claim 1 did not actively recite positive method steps that are sufficiently distinguishable over the cited prior art references. It was advised that claim 1 would more appropriately be presented in combination with the method steps of claims 2 and 3. Such combination of claims 1, 2 and 3 is provided in new claims 11 and 18.

Since an inventive feature of the above-application is to provide a simpler and more streamlined process to making a vertically integrated circuit, options were discussed for amending the claims to make the streamlined process more readily apparent in the claims. Claim 11 is presented to essentially restrict the method to the steps recited therein.

Due to the use of the transitional language of "consisting essentially the steps of" in claim 11, it was recommended that the step of "providing the substrate with active circuit elements via the first side of the substrate" and including the step of etching at least one recess from the second side of the substrate to expose one of the first vertical contacts be included in claim 11. Both of these steps are described and shown in the specification and accompanying figures.

The basic steps of claim 11 are recited in claim 18, however, claim 18 distinguishes the sequence of some of the steps recited therein.

Claim 16 generally recites the subject matter of claim 9 in view of new claim 11. Claim 17 recites the subject matter of claim 10 and is dependent from claim 16.

New claims 12-15 essentially recite parallel subject matter found in original claims 4-7.

It will be noted that claims 1-10 have been cancelled without prejudice or disclaimer.

Acceptance of new claims 11-18 is respectfully requested in the next communication from the Examiner.

3. Rejection of Claim 1 under 35 U.S.C. § 102(b) as being anticipated by U.S. 5,426,072 (Finnila)

Since claim 1 has been canceled, this rejection is now moot.

4. Rejection of Claims 2-5 and 8-10 under 35 U.S.C. § 103(a) as being unpatentable over U.S. 5,426,072 (Finnila)

Rejection of Claim 6 under 35 U.S.C. § 103(a) as being unpatentable over U.S. 5,426,072 (Finnila) in view of Silicon Processing for the VLSI Era (2000) to Wolf et al.

Rejection of Claim 7 under 35 U.S.C. § 103(a) as being unpatentable over U.S. 5,426,072 (Finnila) in view of Semiconductor Manufacturing Technology (2001) to Quirk et al.

As was detailed in the response to the Office Action of May 12, 2003, and further in view of new claims 11, 16 and 18, Finnila discloses a vertically integratable circuit and manufacturing process for making the same that are different than the vertically integratable circuit and manufacturing process for making the same recited in new claims 11, 16 and 18 of the present application.

Firstly, in observing FIGS. 2-5, Finnila describes that an insulating layer 13 for a silicone film 12 is applied before the circuitry 17, 18 of the integrated circuit is provided on the silicone film 12 (col. 3, line 45 through col. 4, line 4). On the other hand, it will be pointed out that insulation elements are provided along a first side of a substrate already bearing vertically integratable circuits in new claims 11 and 18. Since the insulating layer is applied before the circuitry in Finnila, the feedthroughs 16 are also formed before the circuitry is provided. Once again, in the present invention, such feedthroughs or gaps are formed after the circuitry is provided onto the substrate.

Next, Finnila describes a different method for forming the electrically conductive contacts than in claims 11 and 18 of the present application. As shown in FIG. 4, the method of Finnila first includes depositing an electrically conductive member 16a within the feedthroughs. Unlike in the present invention wherein the electroconductive material deposited in the gaps formed in the insulating layer

comprises the electrically conductive contacts for vertical integration, the electrically conductive member 16a according to Finnila does not form the contacts for vertical integration. Instead, as shown in FIG. 5, Finnila further includes the step of depositing another silicone layer 20 over the circuitry 18 and then forming yet another series of openings with metalization 21 deposited therein so as to contact the conductive feedthroughs (col. 4, lines 36-38). After the metalization 21 is formed, an overglass layer is then deposited over the silicone layer 20 and openings are formed in which indium bumps 23 are provided to contact the metalization 21 (col. 4, lines 46-49).

It appears, therefore, that the electrically conductive contacts for vertical integration and of the integrated circuit are not produced in a continuous process, as recited in claim 11 of the present application. This is due to the fact that the indium bumps and the metalizations are formed in a post-production process after the electrically conductive member 16a and the integrated circuit are formed. Accordingly, Finnila describes a method in which the integrated circuit is adapted to be vertically integratable only after it is already formed and is not rendered vertically integratable while it is being formed in a continuous process as recited in claim 1.

As shown in FIG. 7 of Finnila, it appears necessary that the indium bumps 23 be provided on the vertically integratable circuit of Finnila (col. 6, lines 31-36). As indicated in col. 6, lines 34-36, Finnila states that the structure 1 can be any suitable silicone or SOI wafer having circuitry and interconnecting bumps on the top surface. Accordingly, the indium or interconnecting bumps in Finnila are essential to the vertically integratable circuit itself. On the other hand, the method for forming the vertically integratable circuit of the present application recited in claims 11 and 18 does not include the step of forming indium bumps and instead the electrically conductive contacts are formed by only having electroconductive material filled in the gaps formed on the substrate.

In the last Action, the Examiner indicated that method claims of the present application are open for additional processing steps. It will be noted that new claim 11 includes the partially closed terminology "consisting essentially the steps of" to exclude prior art that recites the elements of the claim plus additional elements. Accordingly, such additional processing steps in the disclosure of Finnila are not included in claim 11. Moreover, claim 18 recites the sequence of some of the steps of the method and such sequence is not taught by Finnila.

Claim 16 essentially recites a circuit that is produced by either of the methods of claims 11 and 18, and it is submitted that the disclosure of Finnila does not disclose or suggest the basic circuit of claim 16.

It will be pointed out that the Examiner alleges that the present application fails to establish the criticality of forming vertically integratable circuits prior to the application of the vertical contacts. Applicant respectfully disagrees. Attention should be made to the succinct description in the summary of the invention, which states that the methods of the present application simplify the sequence of production of vertically integratable circuits, and thus the three dimensional integratable circuit as a whole. The simplification of the sequence for production of the circuit optimizes plant running time since numerous process steps are reduced or eliminated. Since finished substrates are no longer the starting point for producing the vertical electric connections, an improved yield is obtained since no process steps which could change the already produced active circuit elements, such as steps with high process temperatures, are necessary any longer after production of the circuit elements (page 2, third full paragraph).

When the present application is considered as a whole, especially in view of the background of the invention and the summary of the invention in the present application, the criticality of providing a substrate bearing vertically integratable circuits prior to providing vertically contacts is readily apparent.

Applicant submits that the disclosures to Wolf et al. and Quirk et al. fail to make up for the basic shortcomings of the disclosure to Finnila described above.

In view of these observations, it is respectfully submitted that the disclosures of Finnila, Wolf et al. and Quirk et al. fail to disclose or suggest the method and circuit of the present application recited in claims 11-18.

5. Conclusion

In view of the new claims, and further in view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is respectfully requested that new claims 11-18 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's Attorney, the Examiner is invited to contact the undersigned at the numbers shown below.

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